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**Experience:**

*Group Leader, CMOS and Novel Devices Group, National Institute of Standards and Technology (NIST), 10/01–present*

- Responsible for technical output, performance, solvency, personnel, and planning for the CMOS and Novel Devices group (CND, <http://www.eeel.nist.gov/812/group06.html>) consisting of approximately 15 staff and associates. The CND group conducts experimental and modeling research related to the measurement and standards infrastructure for CMOS and beyond devices, and their constituent materials as required by the semiconductor industry. This includes Metal-Oxide-Semiconductor (MOS) device characterization and reliability, molecular electronics, silicon nanowires, organic electronics, spectroscopic ellipsometry, scanning capacitance microscopy, and nanofabrication.
- Approximately 1/3 of the CND group budget comes from external and internal competitive sources including International Sematech, DARPA, JPL, NIST Advanced Technology Program, and the NIST Competence Program.
- Supervised research of numerous post-doctoral researchers and graduate students.
- Chair of the 2002 NIST Research Advisory Committee that advises and makes recommendations to the NIST Director on scientific issues, concerns, and opportunities.

*Director, NIST AML (Advanced Measurement Laboratory) Nanofab, 2/03 – 1/06*

- Founding Director of the NIST AML Nanofab which opened in the summer of 2005 and provides researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices. The NF consists of 1000 m<sup>2</sup> of Class 100 clean room space.
- Developed the vision, obtained operating funds, led a cross-laboratory strategic advisory committee, supervise Nanofab staff, and directed the fit-up and start-up process. Presented over 40 overview talks describing the facility to numerous external organizations including NSF, NIH, DARPA, NSA, Defense Dept., and Congressional Staff.

*Researcher, NIST, Semiconductor Electronics Division, 6/98 – present*

- Performed a wide variety of experimental and modeling research on MOS devices, gate dielectric reliability physics, and nanodevices.
- Collaborated with numerous universities and companies including Univ. of Maryland, North Carolina State Univ., IBM and SEMATECH.

*Research Assistant, North Carolina State University, 6/94 – 6/98*

- Performed research and wrote thesis on aspects related to characterization, modeling, fabrication, and development of rapid thermal chemical vapor deposited oxynitride

dielectrics for use as a gate insulator in advanced MOS devices. Advisor: Dr. J. J. Wortman, ECE.

- Co-taught a graduate level physical electronics class in the electrical engineering department.

**Education:**

- Ph. D. in Electrical Engineering (8/98) - North Carolina State University
- M. S. in Electrical Engineering (5/96) - North Carolina State University
- B. S. in Electrical Engineering (5/94) - Pennsylvania State University

**University Memberships:**

- Adjunct Faculty Member North Carolina State University, 4/99 – present, faculty committee member of Chad Weintraub (Ph.D., 8/00) and Heather Lazar (Ph. D., exp. 5/05)
- Special Faculty Member University of Maryland, Research Advisor of Da-wei Heh (Ph. D., May, 2005)

**Industry Committees:**

- International Technology Roadmap for Semiconductors, Emerging Research Materials Working Group, 3/04 - present
- International Technology Roadmap for Semiconductors, Front-End Processes Technical Working Group, 5/00 – 3/04
- SEMATECH Reliability Engineering Working Group, 11/98 – 11/01
- SEMATECH Gate Stack Engineering Working Group, 11/98 – 11/01

**Conference Committees:**

- Workshop on Dielectrics in Microelectronics Program Committee, 11/02 – present
- IEEE Semiconductor Interface Specialists Conference, Executive Committee (2003 Arrangements Chair, 2004 Technical Chair, 2005 General Chair, 2006 Ex-Officio Chair)
- IEEE Semiconductor Interface Specialists Conference Program Committee, 1/00 – 1/03
- IEEE 2001 International Reliability Physics Symposium Dielectrics Program Co-chair
- IEEE International Reliability Physics Symposium Dielectrics Program Committee, 10/00 – 9/03
- IEEE Integrated Reliability Workshop Technical Program Committee, 5/01 – 9/03
- Co-organizer MRS Workshop on High- $\kappa$  Gate Dielectrics, June 1-2, 2000

**Society Memberships:**

- Institute of Electrical and Electronics Engineers, Materials Research Society, American Physical Society

**Book Chapters and Tutorials:**

6. E. M. Vogel, ‘Electrical Characterization of MOS Devices with Advanced Gate Stacks,’ Tutorial, 2005 MIGAS International School on Advanced Microelectronics, Physical and Electrical Characterization of Materials and Devices for Silicon Nanoelectronics, (<http://www.migas.inpg.fr/>), Grenoble, France, June 11-17, 2005.

5. E. M. Vogel, 'Characterization, Physical Modeling, and Assessment of Gate Oxide Reliability,' Tutorial, 2002 IEEE International Reliability Physics Symposium, Dallas, TX, April 7, 2002.
4. E. M. Vogel, and V. Misra, 'MOS Device Characterization,' in *Handbook of Silicon Semiconductor Metrology*, Marcel-Dekker, ed. A. C. Diebold, pp. 59-96, 2001.
3. E. M. Vogel, 'Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment,' Tutorial, 2001 IEEE Integrated Reliability Workshop, Lake Tahoe, CA, Oct. 15, 2001.
2. C. R. Cleavelin, S. Pas, E. M. Vogel, and J. J. Wortman, 'Oxidation,' in *Handbook of Semiconductor Manufacturing Technology*, Marcel-Dekker, ed. Y. Nishi, and R. Doering, 2000.
1. J. S. Suehle and E. M. Vogel, 'Thin Gate Oxide Reliability,' Tutorial, International Reliability Physics Symposium, Apr. 10, 2000.

**Journal Publications:**

41. C. A. Richter, C. A. Hacker, L. J. Richter, O. A. Kirillov, J. S. Suehle, and E. M. Vogel, "Interface Characterization of Molecular-Monolayer/SiO<sub>2</sub> Based Molecular Junctions," submitted to *Sol. St. Elecs.*
40. D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, G. Bersuker, P. Y. Hung, and A. Diebold, "Electrical Characterization of Spatial Distributions of Trapping Centers in HfO<sub>2</sub>/SiO<sub>2</sub> Gate Stack," submitted to *IEEE Trans. Elec. Dev.*
39. S.-E. Park, J. S. Suehle, J. J. Kopanski, E. M. Vogel, and A. Davydov, "Determination of work functions for metals by scanning Kelvin probe microscopy", submitted to *J. Appl. Phys.*
38. S.-E. Park, J. S. Suehle, J. J. Kopanski, and E. M. Vogel, "Calibration of work function for Pt<sub>0.95</sub>Ir<sub>0.05</sub> films with scanning Kelvin probe microscopy," submitted to *Appl. Phys. Lett.*
37. D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, P. Y. Hung, and A. Diebold, G. Bersuker, "Spatial Distributions of Trapping Centers in HfO<sub>2</sub>/SiO<sub>2</sub> Gate Stacks," accepted *Appl. Phys. Lett.*
36. S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures," *J. Vac. Sci Tech. B*, vol. 24, p. 404, 2006.
35. J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, C. Young, S. Shah, D. Maher, B. Foran, P. Y. Hung, and A. Diebold, "A Comparison of Thickness Values for Very Thin SiO<sub>2</sub> Films by Using Ellipsometric, Capacitance-Voltage, and HRTEM Measurements," *Journal of the Electrochemical Soc.*, vol. 153, p. F12, 2006.

34. S.-M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel, "Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors", *NanoLetters*, vol. 5, p. 2519, 2005.
33. S.-M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, and E. M. Vogel, "Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors," *Nanotechnology*, vol. 16, p. 1482, 2005.
32. G. K. Ramachandran, M. D. Edelstein, D. L. Blackburn, J. S. Suehle, E. M. Vogel, and C. A. Richter, "Nanometre gaps in gold wires are formed by thermal migration," *Nanotechnology*, vol. 16, p. 1294, 2005.
31. J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, and J. S. Suehle, 'Reverse Short Channel Effects in High-k gated nMOSFETs,' *Microelectronics Reliability*, vol. 45, p. 783, 2005.
30. S.-M. Koo, A. Fujiwara, J.-P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High Inversion Current in Silicon Nanowire Field Effect Transistors," *NanoLetters*, vol. 4, p. 2197, 2004.
29. N. V. Nguyen, J. E. Maslar, Jin-Yong Kim, Jin-Ping Han, Jin-Won Park, D. Chandler-Horowitz, and E. M. Vogel, "Crystalline Quality of Silicon-On-Insulator Characterized by Spectroscopic Ellipsometry and Raman Spectroscopy," *Appl. Phys. Lett.*, vol. 85, p. 2765, 2004.
28. J.-P. Han, S.-M. Koo, C. A. Richter, and E. M. Vogel, "Influence of buffer layer thickness on memory effects of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub>/SiN/Si structures", *Appl. Phys. Lett.*, vol. 85, pp. 1439-1441, 2004.
27. C. A. Richter, C. Hacker, L. J. Richter, E. M. Vogel, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon", *Solid State Electronics*, vol. 48, pp. 1747-1752, 2004.
26. J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- and p-MOSFETs with HfO<sub>2</sub> Gate Dielectric on Ultrathin SiON Buffer Layer," *IEEE Electron Dev. Lett.*, vol. 25, p. 126, 2004.
25. E. M. Vogel, C. A. Richter, and B. G. Rennex, 'A capacitance-voltage model for polysilicon-gated MOS devices including substrate quantization effects based on modification of the total semiconductor charge,' *Sol.-St. Elecs.*, vol. 47, p. 1589, 2003.
24. D.-W. Heh, E. M. Vogel, and J. B. Bernstein, 'Impact of Substrate Hot Hole Injection on Ultra-thin Silicon Dioxide Breakdown,' *Appl. Phys. Lett.*, vol. 82, p. 3242, 2003.
23. E. M. Vogel, D.-W. Heh, and J. B. Bernstein, 'Impact of the Trapping of Anode Hot Holes on Silicon Dioxide Breakdown,' *IEEE Elec. Dev. Lett.*, vol. 23, p. 667, 2002.
22. E. M. Vogel, D. Heh, and J. B. Bernstein, 'Interaction between low energy electrons and defects created by hot holes in ultra-thin silicon dioxide,' *Appl. Phys. Lett.*, vol. 80, p. 3343, 2002.

21. J. S. Suehle, E. M. Vogel, P. Roitman, J. F. Conley, Jr., A. H. Johnston, B. Wang, J. B. Bernstein, and C. E. Weintraub, 'Observation of Latent Reliability Degradation in Ultra-Thin Oxides After Heavy-Ion Irradiation,' *Appl. Phys. Lett.*, vol. 80, p. 1282, 2002.
20. J. F. Conley, Jr., J. S. Suehle, A. H. Johnston, B. Wang, T. Miyahara, E. M. Vogel, and J. B. Bernstein, 'Heavy Ion Induced Soft Breakdown of Thin Gate Oxides,' *IEEE Trans. Nucl. Sci.*, vol. 48, p. 1913, 2001.
19. C. E. Weintraub, E. M. Vogel, N. Yang, V. Misra, J. J. Wortman, J. J. Ganem, and P. Masson, 'Application of Low Frequency Charge Pumping on Thin Stacked Dielectrics,' *IEEE Trans. Elec. Dev.*, vol. 48, p. 2754, 2001.
18. E. M. Vogel, M. D. Edelstein, and J. S. Suehle, 'Reliability of Ultra-thin Silicon Dioxide Under Substrate Hot-electron, Substrate Hot-hole, and Tunneling Stress,' *Microelectronic Engineering*, vol. 59, p. 73, 2001.
17. E. M. Vogel, M. D. Edelstein, and J. S. Suehle, 'Defect generation and breakdown of ultra-thin silicon dioxide induced by substrate hot-hole injection,' *J. Appl. Phys.*, vol. 90, p. 2338, 2001.
16. B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, 'Time-Dependent Breakdown of Ultra-Thin SiO<sub>2</sub> Gate Dielectrics Under Pulsed Biased Stress,' *IEEE Elec. Dev. Lett.*, vol. 22, p. 224, 2001.
15. C. A. Richter, A. R. Hefner, and E. M. Vogel, 'A Comparison of Quantum-Mechanical Capacitance-Voltage Simulators,' *IEEE Elec. Dev. Lett.*, vol. 22, p. 35, 2001.
14. W. K. Henson, N. Yang, S. Kubicek, E. M. Vogel, J. J. Wortman, K. De Meyer, and A. Naem, 'Analysis of Leakage Currents and Power Consumption for CMOS Technology in the 100 nm Regime,' *IEEE Trans. Elec. Dev.*, vol. 47, p.1393, 2000.
13. E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein, 'Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress,' *IEEE Trans. Elec. Dev.*, vol. 47, p. 1183, 2000.
12. E. M. Vogel, W. K. Henson, C. A. Richter, and J. S. Suehle, 'Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics,' *IEEE Trans. Elec. Dev.*, vol. 47, p. 601, 2000.
11. A. Shanware, H. Z. Massoud, E. Vogel, K. Henson, J. R. Hauser, and J. J. Wortman, 'Modeling the Trends in Valence-Band Electron Tunneling in NMOSFETs with Ultrathin SiO<sub>2</sub> and SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> Dielectrics with Oxide Scaling,' *Microelectronic Eng.*, vol. 48, p. 295, 1999.
10. P. Masson, P. Morfouli, J. L. Autran, J. Brini, B. Balland, E. M. Vogel, and J. J. Wortman, 'Electrical Properties of Oxynitride Thin Films Using Noise and Charge Pumping Measurements,' *Journal of Non-Crystalline Solids*, vol. 245, p. 54, 1999.

9. W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. Datta, M. Xu and D. Venables, 'Estimating Oxide Thickness of Tunnel Oxides Down to 1.4 nm Using Conventional Capacitance-Voltage Measurements on MOS Capacitors,' *IEEE Elect. Dev. Lett.*, vol. 20, p. 179, 1999.
8. V. Z-Q. Li, M. R. Mirabedini, E. Vogel, K. Henson, D. Batchelor, J. J. Wortman, and R. T. Kuehn, 'Effects of Si Source Gases (SiH<sub>4</sub> and Si<sub>2</sub>H<sub>6</sub>) on Polycrystalline-Si<sub>1-x</sub>Ge<sub>x</sub> Deposited on Oxide by RTCVD,' *Electrochemical and Solid-State Letters*, vol. 1, p. 153, 1998.
7. E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, 'Modeled tunnel currents for high dielectric constant dielectrics,' *IEEE Trans. Elect. Dev.*, vol. 45, pp.1350-1355, 1998.
6. P. Morfouli, G. Ghibaud, E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, and J. J. Wortman, 'Electrical and reliability properties of thin silicon oxynitride dielectrics formed by low pressure rapid thermal chemical vapor deposition' *Sol.-St. Elecs.*, vol. 41, p. 1051, 1997.
5. P. Morfouli, G. Ghibaud, T. Ouisse, E. Vogel, W. Hill, V. Misra, P. McLarty, and J. J. Wortman, 'Low-frequency noise characterization of n- and p- MOSFET's with ultrathin oxynitride gate films,' *IEEE Elect. Dev. Lett.*, vol. 17, pp. 395-397, 1996.
4. E. M. Vogel, W. L. Hill, V. Misra, P. K. McLarty, J. J. Wortman, J. R. Hauser, P. Morfouli, G. Ghibaud, and T. Ouisse, 'Mobility behavior of n-channel and p-channel MOSFETs with oxynitride gate dielectrics formed by low-pressure rapid thermal chemical vapor deposition,' *IEEE Trans. Elec. Dev.*, vol. 43, pp. 753-758, 1996.
3. V. Misra, W. K. Henson, E. M. Vogel, G. A. Hames, P. K. McLarty, J. R. Hauser, and J. J. Wortman, 'Electrical properties of composite gate oxides formed by rapid thermal processing,' *IEEE Trans. Elec. Dev.*, vol. 43, pp. 636-646, 1996.
2. W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty, and J. J. Wortman, 'Low-pressure rapid thermal chemical vapor deposition of oxynitride gate dielectrics for n-channel and p-channel MOSFETs,' *IEEE Trans. Elec. Dev.*, vol. 43, pp. 15-22, 1996.
1. W. L. Hill, E. M. Vogel, P. K. McLarty, V. Misra, J. J. Wortman, and V. Watt, 'N-channel and p-channel MOSFETs with gate dielectrics formed using low pressure rapid thermal chemical vapor deposition,' *Microelectronic Eng.*, vol. 28, p. 269, 1995.

**Conference Presentations with Proceedings (5 Invited\*):**

21. C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B.H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker, "Detection of Electron Trap Generation Due to Constant Voltage Stress on High- $\kappa$  Gate Stacks," accepted 2006 International Reliability Physics Symposium.

- \*20. E. M. Vogel, 'Characterization of electrically active defects in high-k gate dielectrics using charge pumping,' NATO Advanced Research Workshop on Defects in Advanced High-k Dielectrics, St. Petersburg, Russia, July 11-14, 2005.
- \*19. E. M. Vogel, 'Physical Mechanisms of Ultra-thin Silicon Dioxide Degradation and Breakdown,' 8th International Symposium on Silicon Nitride, Silicon Dioxide Thin Insulating Films and Other Emerging Dielectrics, 207th Electrochemical Society meeting, Quebec City, Canada, May 15-20, 2005
18. B. Zhu, J. S. Suehle, E. Vogel, and J. B. Bernstein, 'The Contribution of HfO<sub>2</sub> Bulk Oxide Traps to Dynamic NBTI in pMOSFETs,' IEEE International Reliability Physics Symposium, San Jose, CA, April 17-20, 2005.
- \*17. E. M. Vogel, 'Metrology for Emerging Research Devices and Materials,' International Conference on Characterization and Metrology for ULSI Technology, Univ. Texas-Dallas, Richardson, Texas, March 15-18, 2005.
16. N. V. Nguyen, J. E. Maslar, J.-Y. Kim, J.-P. Han, J.-W. Park, D. Chandler-Horowitz, and E. M. Vogel, 'Characterization of Structural Quality of Bonded Silicon-on-Insulator Wafers by Spectroscopic Ellipsometry and Raman Spectroscopy,' Materials Research Society Spring Meeting, High-Mobility Group-IV Materials and Devices, B8.19, San Francisco, CA, April, 2004.
15. D. Heh, E. M. Vogel, and J. B. Bernstein, "New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides," Integrated Reliability Workshop, Fallen Leaf Lake, CA, Oct. 20, 2004.
14. J.-P. Han, E. M. Vogel, E.P. Gusev, C. D'Emic, C.A. Richter, D. W. Heh, J. Suehle, 'Energy Distribution of Interface Traps in High-k Gated MOSFETs,' 2003 Symposium on VLSI Tech. Digest of Technical Papers, Kyoto, Japan, June 12, 2003.
- \*13. E. M. Vogel, and G. A. Brown, 'Challenges of Electrical Measurements of Advanced Gate Dielectrics in Metal-Oxide-Semiconductor Devices,' 2003 International Conference on Characterization and Metrology for ULSI Technology, Austin, TX, March 27, 2003.
12. J. Ehrstein, C. Richter, D. Chandler-Horowitz, E. Vogel, D. Ricks, C. Young, S. Spencer, S. Shah, D. Maher, B. Foran, A. Diebold, and P. Y. Hung, 'Thickness evaluation for 2 nm SiO<sub>2</sub> films, a comparison of ellipsometric, capacitance-voltage and HRTEM measurements,' 2003 International Conference on Characterization and Metrology for ULSI Technology, Austin, TX, March 27, 2003.
- \*11. E. M. Vogel, 'Issues with Electrical and Reliability Characterization of Advanced Gate Dielectrics,' Proceedings of the 12<sup>th</sup> Workshop on Dielectrics in Microelectronics, Grenoble, France, Nov. 20, 2002.

10. D. Heh, J. B. Bernstein, E. M. Vogel, 'Defect Generation in Ultra-thin Oxide Over Large Fluence Ranges,' 2002 IEEE Integrated Reliability Workshop Final Report, Lake Tahoe, CA, Oct. 21-23, 2002.
9. B. Wang, J. S. Suehle, J. F. Conley, Jr., E. M. Vogel, C. E. Weintraub, A. H. Johnston, and J. B. Bernstein, 'Latent Reliability Degradation of Ultra-Thin Oxides After Heavy Ion and  $\gamma$  -ray Irradiation,' 2001 IEEE Integrated Reliability Workshop Final Report, Lake Tahoe, CA, Oct. 15-18, 2001.
8. B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, "The Effect of Stress Interruption and Pulsed Bias Stress on Ultra-thin Gate Dielectric Reliability," 2000 IEEE International Integrated Reliability Workshop Final Report, Lake Tahoe, CA, Oct. 23-26, 2000.
7. J. S. Suehle, E. M. Vogel, B. Wang, J. B. Bernstein, 'Temperature Dependence of Soft Breakdown and Wear-Out in Sub 3 nm SiO<sub>2</sub> Films' Proceedings of the 2000 International Reliability Physics Symposium, p. 33, 2000.
6. A. Shanware, J. P. Shiely, H. Z. Massoud, E. Vogel, K. Henson, A. Srivastava, C. Osburn, J. R. Hauser, and J. J. Wortman, 'Extraction of the Gate Oxide Thickness of N- and P-Channel MOSFETs Below 20 Å from the Substrate Current Resulting from Valence-Band Electron Tunneling,' Proceedings of the 1999 International Electron Device Meeting, Washington, DC, December 5-8, 1999.
5. A. Shanware, H. Z. Massoud, E. Vogel, K. Henson, J. R. Hauser, and J. J. Wortman, 'Comparison of Valence-Band Tunneling in Pure SiO<sub>2</sub>, Composite SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub>, and Pure Ta<sub>2</sub>O<sub>5</sub>, in MOSFETs with 1.0 nm-Thick SiO<sub>2</sub>-Equivalent Gate Dielectrics,' Proceedings of the 1999 Materials Research Society Spring Meeting, San Francisco, CA, Apr. 5-8, 1999.
4. R. A. Allen, E. M. Vogel, L. W. Linholm, and M. W. Cresswell, 'Sheet and Line Resistance of Patterned SOI Surface Film CD Reference Materials as a Function of Substrate Bias,' Proceedings of the 1999 IEEE International Conference on Microelectronic Test Structures, Goteborg, Sweden, March 15-18, 1999.
3. A. Srivastava, H. H. Heinisch, E. Vogel, C. Parker, C. M. Osburn, N. A. Masnari, J. J. Wortman, and J. R. Hauser, 'Evaluation of 2.0 nm Grown and Deposited Dielectrics in 0.1  $\mu$ m PMOSFETs,' Proceedings of the 1998 MRS Spring Symposium, San Francisco, CA, Apr 13-15, 1998.
2. P. Morfouli, G. Ghibaud, E. M. Vogel, W. L. Hill, V. M. Misra, P. K. McLarty, and J. J. Wortman, 'Electrical and Reliability Properties of Thin Silicon Oxynitride Dielectrics Formed by Low Pressure Rapid Thermal Chemical Vapor Deposition,' Proceedings of the 7<sup>th</sup> ESPRIT Workshop on Dielectrics in Microelectronics, Crete, Greece, November, 1995.
1. P. Morfouli, G. Ghibaud, T. Ouisse, E. M. Vogel, W. L. Hill, V. Misra, P. McLarty, J. J. Wortman, 'Noise Analysis of MOSFET's with Ultra Thin Silicon Oxynitride Films Prepared by

Low Pressure Rapid Thermal Chemical Vapor Deposition (LPRTCVD)', Proceedings of the 25<sup>th</sup> European Solid State Device Research Conference, Hague, Netherlands, September 25-27, 1995.

**Conference and Other Presentations (20 Invited\*):**

39. S.-E. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures", 2005 Ultra Shallow Junction Conference, Daytona Beach, FL.

38. S.-E. Park, St. Jeliaskov, J. J. Kopanski, J. Suehle, E. Vogel, A. Davydov, and H.-K. Shin, "Electrical Characterization of MOS structures and Wide Bandgap Semiconductors by Scanning Kelvin Probe Microscopy", 2005 MRS Spring Meeting, San Francisco, CA.

37. M. Green and E. M. Vogel, "Method for Measuring the Barrier Height at the High-k/Metal Electrode Interface, and Combinatorial Determination of Optimal Metal Gate Electrodes," SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 14, 2005.

\*36. E. M. Vogel and D. Heh, "Depth Profiles of Electrically Active Defects in High-k Gate Stacks Using Charge Pumping," SEMATECH Advanced Gate Stack Engineering Working Group Biannual Meeting, Austin, TX, Feb. 15, 2005.

\*35. E. M. Vogel, 'A Perspective on the Future of Electronics,' Nano 2004, Baltimore, MD, Nov. 12, 2004.

\*34. Eric M. Vogel, "Characterization Needs for Emerging Research Materials and Devices," ITRS Emerging Research Materials Workshop, San Francisco, CA, July 11, 2004.

33. J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, J. S. Suehle, "Reverse Short Channel Effects in High-k Gated nMOSFETs," 13<sup>th</sup> Workshop on Dielectrics in Microelectronics, Kinsale, Ireland, June 28, 2004.

\*32. Curt A. Richter and Eric Vogel, "Computational Needs for Emerging Materials: An Experimental Metrologist's Viewpoint", Materials Modeling for Emerging Research Materials Workshop, Austin, TX, June 7, 2004.

31. Jin-Ping Han, S.M. Koo, C. A. Richter and Eric Vogel, "Influence of Buffer Layer Thickness on the Ferroelectric Memory window of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub>/SiN/Si Structure", 16th international Symposium on Integrated Ferroelectrics (ISIF'04), Gyeongju, Korea, April 5-8, 2004.

\*30. E. M. Vogel, "Challenges of Electrical Measurements of Advanced Gate Dielectrics in MOS Devices," Applied Materials, Feb. 9, 2004.

29. J. Park, C. A. Richter, J. Y. Kim, N. V. Nguyen, J. E. Bonevich, and E. M. Vogel, 'Characterization of ultrathin amorphous silicon and correlation with crystalline evolution after thermal annealing,' 2003 MRS Spring Meeting.

\*28. E. M. Vogel, 'Issues with Electrical and Reliability Characterization of Advanced Gate Dielectrics,' 5<sup>th</sup> Topical Research Conference on Reliability, Austin, TX, Oct. 28, 2002.

\*27. E. M. Vogel and D. Blackburn, 'NIST Response to ITRS and Beyond,' SRC Metrology Needs for Emerging Technologies Workshop, Raleigh, NC, May 3, 2002.

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